

## **CLAIMS**

## What is claimed is:

1. A transistor circuit for implementing a switch, comprising:

- a first switch node configured to connect to an external circuit;
- a second switch node configured to connect to the external circuit;
- a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
  - a third switch node for receiving the control signal; and
- a circuit connected to the third switch node and the third terminal of the transistor device, the circuit having an impedance configured to reduce the parasitic capacitance of the transistor device.
- 2. The circuit of claim 1, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.
- 3. A transistor circuit for implementing a switch, comprising:
  - a first switch node configured to connect to an external circuit;
  - a second switch node configured to connect to the external circuit;
- a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal, and
- a circuit connected to the second terminal of the transistor device, the circuit configured to provide a voltage to the second terminal when the control signal engages the transistor device.



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- 4. The circuit of claim 3, wherein the transistor device is a metal-oxide-semiconductor field-effect transistor.
- 5. The circuit of claim 3, wherein the circuit is an inverter circuit.

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- 6. A transistor circuit for implementing a differential switch, comprising:
  - a first switch node configured to connect to an external circuit;
  - a second switch node configured to connect to the external circuit;
- a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device having a first terminal connected to the third terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and

a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal.

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The transistor circuit of claim 6, wherein the first transistor device, the second transistor device, and the third transistor device are each a metal-oxide-semiconductor field-effect transistor.

8. The circuit of claim 6, wherein the first transistor, the second transistor, and the third transistor are configured in a predetermined manner so that the parasitic characteristics of the first transistor, the second transistor, and the third transistor result in the transistor circuit having predetermined parasitic characteristics.

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